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Area-Delay Efficient Binary Adders in QCA

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ABSTRACT
In this paper, a novel quantum-dot cellular automata (QCA) adder design is presented that decrease the number of QCA cells compared to previously method designs. The proposed one-bit QCA adder is based on a new algorithm that requires only three majority gates and two inverters for the QCA addition. A novel 128-bit adder designed in QCA was implemented. It achieved speed performances higher than all the existing. QCA adders, with an area requirement comparable with the low RCA and CFA established. The novel adder operates in the RCA functional, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In adding together, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the explanation was limited. As transistors reduce in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot find much smaller than their current size. The quantum-dot cellular automata approach represents one of the possible solutions in overcome this physical limit, even though the design of logic modules in QCA is not forever straightforward.

Keywords- Adders, nano-computing, QCA (quantum-dot cellular automata)

I. INTRODUCTION

In this paper, a new QCA adder design is implemented that reduces the number of QCA cells when compared to Existing reported designs. We demonstrate that it is possible to design a CLA QCA one-bit adder, with the same reduced hardware as the bit-serial adder, as retaining the simpler clocking scheme and parallel structure of the novel CLA approach. The proposed design is based on a new algorithm that requires only three majority gates and two inverters for the QCA addition. It is noted that the bit-serial QCA adder uses a variant of the proposed one-bit QCA adder. By connect *n* proposed one-bit QCA adders..

A quantum-dot cellular automaton (QCA) is an attractive emerging technology suitable for the development of ultra dense low-power higher-performance digital circuits. For this cause in the last few years, the design of proficient logic circuits in QCA has received a great deal of attention. Special efforts are directed to arithmetic circuits, with the major interest focused on the binary addition that is the basic operation of any digital system. Of course,The designs commonly employed in traditional CMOS designs are considered a first reference for the new design environment. Ripple-carry, carry look-ahead (CLA), and conditional sum adders were implemented in. The carry-flow adder shown in was mainly an improved RCA in which detrimental wires effects were mitigated. Parallel-prefix architectures, including Brent–Kung (BKA), Kogge–Stone, Ladner–Fischer, and Han–Carlson adders, were analyzed and implemented in QCA.

Recently, further efficient designs were proposed for the CLA and the BKA, and for the CLA and the CFA. In this brief, an innovative technique is presented to implement high-speed low-area adders into QCA. Theoretical formulations established for CLA and parallel-prefix adders are here exploited for the realize of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, those avoiding unnecessary clock phases due to long interconnections.

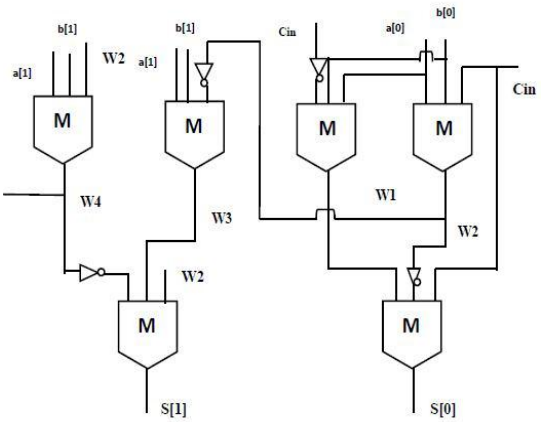


Fig 1 Novel 2-bit basic module

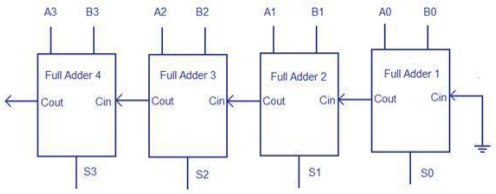
An adder designed as proposed runs in the RCA fashion, but it exhibit a computational delay lower

than all state-of theatre competitors and achieves the lowest area-delay product (ADP).

II. REGULAR METHOD

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A RCA is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. A propagation delay inside the logic circuitry is the reason behind this. Propagation delay is time between the application of an input and occurrence of the corresponding output.

Consider a NOT gate, When the input is "0″ the output will be "1″ and vice versa. The time taken for the NOT gate's output to become "0″ after the application of logic "1″ to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (Cout) signal.



RCA architecture

Basic Full adder block

To understand the working of a ripple carry adder completely, you need to have a look at the full adder too. Full adder is a logic circuit that adds two input operand bits plus a Carry in bit and outputs a Carry out bit and a sum bit.. The Sum out (Sout) of a full adder is the XOR of input operand bits A, B and the Carry in (Cin)bit. Truth table and schematic of a 1 bit Full adder is shown below There is a simple trick to find results of a full adder. Consider the second last row of the truth table, here the operands are 1, 1, 0 ie (A, B, Cin). Add them together ie 1+1+0 = 10 . In binary system, the number order is 0, 1, 10, 11……. and so the result of 1+1+0 is 10 just like we get 1+1+0 =2 in decimal system. 2 in the decimal system correspond to 10 in the binary system. Swapping the result "10″ will give S=0 and Cout = 1 and the second last row is justified..

Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

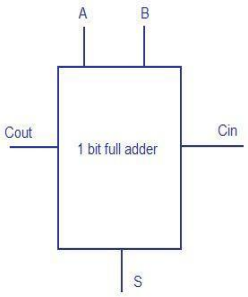


Fig ; 1 bit full adder schematic and truth table

III. PROPOSED METHOD

A QCA is a nano-structure having as its basic cell a square four quantum dots structure charged with two free electrons able to tunnel through the dots inside the cell. Because of Columbic repulsion, the two electrons will forever reside in opposite corners. The locations of the electrons in the cell determine two possible stable states that can be associated to the binary state 1 and 0.

Cell Design

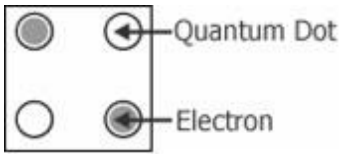


Fig: Simplified Diagram of QCA Cell

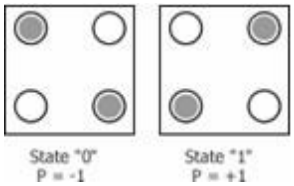


Fig :Four Dot Quantum Cell

Structure of Majority gate

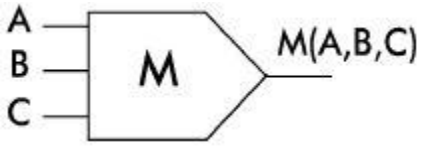


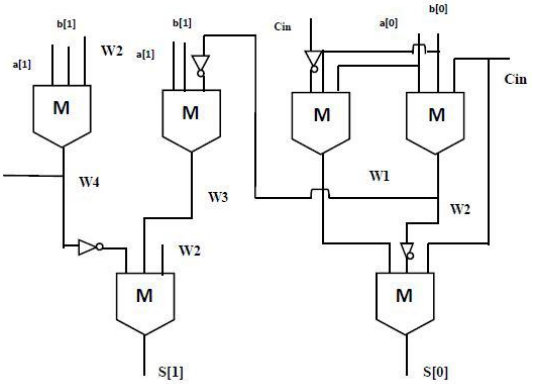
Fig: Structure of Majority gate

QCA Majority Gate:

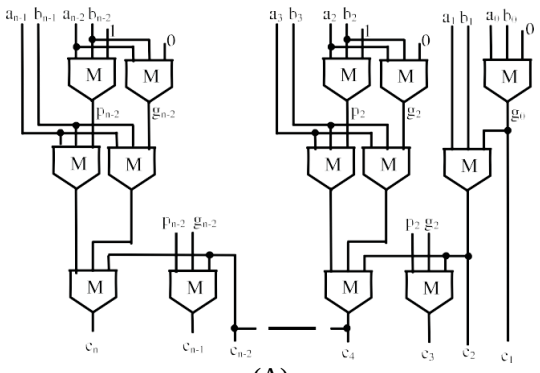
The QCA majority gate performs a three-input logic function. Assuming the inputs are A ,B and C, the logic function of the majority gate is

$$M = AB+BC+CA$$

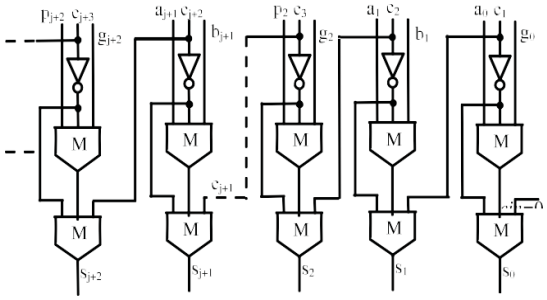
Architecture of Basic Novel 2-bit adder



Although adjacent cells interact through electrostatic forces and tend to arrange in a line their polarizations, QCA cells do not have intrinsic data flow directionality. To achieve controllable data directions, the cells inside a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90°. This clock system named the zone clocking scheme, makes the QCA designs intrinsically pipelined, as each clock zone behaves like a D-latch. QCA cells are used for both logic designs and interconnections that can exploit either the coplanar cross or bridge technique. The fundamental logic gates inherently available within the QCA technology are the inverter and the MG. Given three inputs *a*, *b*, and *c*, the MG perform the logic function reported in (1) provided that all input cells are associated to the same clock signal clk*x*(with *x* ranging from 0 to 3), whereas the remaining cells of the MG are linked to the clock signal clk*x*+1



(A)



(b)

Fig. 2. Novel *n*-bit adder (a) carry chain and (b) sum block.

With the main objective of trading off area and delay, the hybrid adder (HYBA) described in [14] combines a parallel-prefix adder with the RCA. In the presence of *n*-bit operands, this architecture has a worst computational path consisting of 2×log2 *n* +2 cascaded MGs and one inverter. When the methodology recently proposed in [15] was exploited, the worst case path of the CLA is reduced to 4 × _log4 *n*_ + 2 × _log4 *n*_ − 1 MGs and one inverter. The above-mentioned approach can be applied also to design the BKA. In this case the overall area is reduced with respect to [13], but maintaining the same computational path. By applying the decomposition method demonstrated in [16], the computational paths of the CLA and the CFA are reduced to 7 + 2×log2*(n/8)* MGs and one inverter and to *(n/2)*+ 3 MGs and one inverter, respectively.

IV. NOVEL QCA ADDER

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two *n*-bit addends *A* = *an*−1, . . . , *a*0 and *B* = *bn*−1, . . . , *b*0 and suppose that for the *i*th bit position (with *i* = *n* − 1, . . . , 0) the auxiliary propagate and generate signals, namely *pi* = *ai* + *bi* and *gi* = *ai* · *bi* , are computed.*ci* being the carry produced at the generic *(i*−1)th bit position, the carry signal *ci*+2, furnished at the (*i*+1)th bit position, can be computed using the conventional CLA logic reported in (2). The latter can be rewritten as given in (3), by exploiting Theorems 1 and *2* demonstrated in [15]. In this way, the RCA action, needed to propagate the carry *ci* through the two

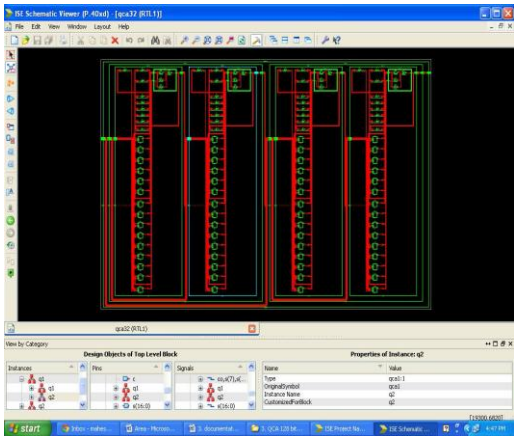


Fig. 3. Novel 32-bit adder.

Novel 64-bit adder

Subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.

Equation (3) is exploited in the design of the novel 2-bit module shown in Fig. 1 that also shows the computation of the carry $ci+1 = M(pi\ gi\ ci)$. The proposed n-bit adder is then implemented by cascading $n/2$ 2-bit modules as shown in Fig. 2(a). Having assumed that the carry-in of the adder is $cin = 0$, the signal $p0$ is not required and the 2-bit module used at the least significant bit position is simplified. The sum bits are finally computed as shown in
Fig. 2(b).

It must be noted that the time critical addition is performed when a carry is generated at the least significant bit position (i.e., g0 = 1) and then it is propagated through the subsequent bit positions to the most significant one. In this case, the first 2-bit module computes $c2$, contributing to the worst case computational path with two cascaded MGs. The subsequent 2-bit modules contribute with only one MG each, thus introducing a total number of cascaded MGs equal to $(n - 2)/2$. Considering that further two MGs and one inverter are required to compute the sum bits, the worst case path of the novel adder consists of $(n/2) + 3$ MGs and one inverter.

$$ci+2 = gi+1 + pi+1 \cdot gi + pi+1 \cdot pi \cdot ci \quad (2)$$

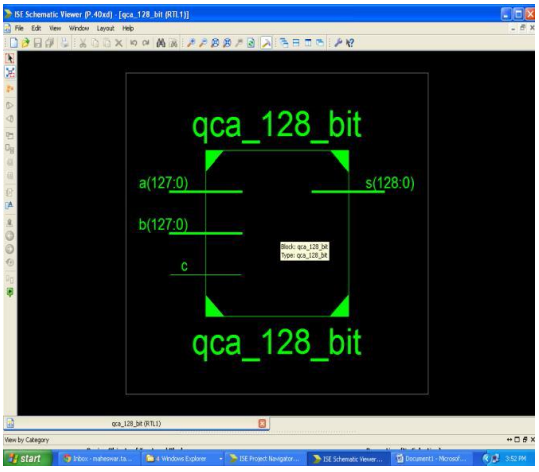
$$ci+2 = M(M\_ai+1, bi+1, gi \quad M\_ai+1, bi+1, pi \quad ci). \quad (3)$$

Obtained from the FCP block are passed through another set of multiplexers, where one control parameter (INTP_SEL) selects the desired filter depending on the interpolation factor. This technique reduces the total number of filter coefficients that will be processed further from the earlier requirement of 111–49 after the FCP. Combination of FCP and SCP steps reduces the requirement of MPIS from 42 to 7 and APIS from 36 to 6, which facilitates 83.3% improvement for this design. According to the proposed method, considering more filters of different specifications will cause more reduction in the APIS and MPIS.

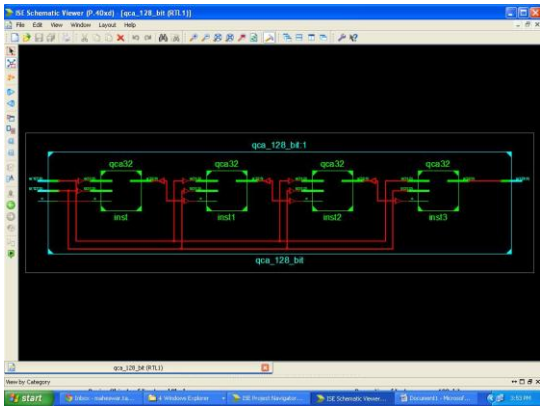
V. RESULTS

The proposed addition design is implemented for several operands word lengths using the QCA Designer tool adopting the same rules and simulation settings used.

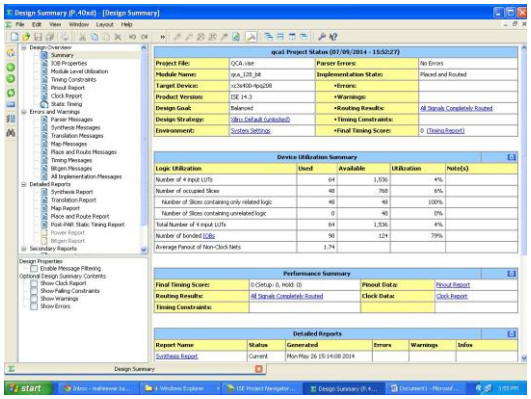
Block diagram



RTL schematic



Design summary



Simulation output

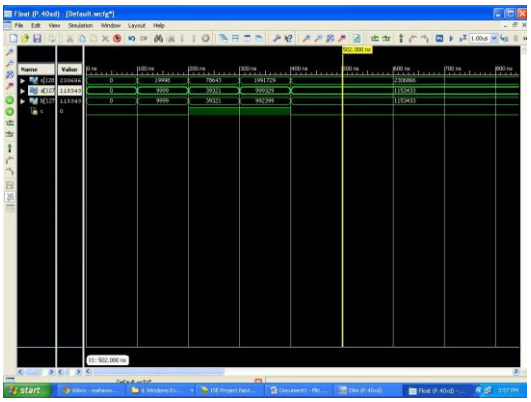


Fig. 6. Simulation results obtained for the novel 128-bit adder.

VI. CONCLUSION

A new adder designed in QCA was implemented. It achieved speed performances high than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lesser than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the explanation was limited. A 128-bit binary adder designed as described in this brief.

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